MCGREP

A Predictable Architecture for Embedded Real-Time Systems

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Overview

- A real-time problem,
- The proposed solution and its features,
- Initial implementation and experiments,
- Results,
- Conclusion and future work.

A Real-Time Problem

We always need more computing power!

Requirements for a processor for a **real-time** system:

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  (run more demanding applications)

These conflict!

A Processor

Parallel problem: Portable embedded devices have limited electrical power.

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These also conflict!

Our Problem

Real-time systems need the following in the future:

- Low Power Consumption
  (conserve battery life)
- Predictability
  (ensure correctness)
- Execution Speed
  (run more demanding applications)

Custom Hardware

Application-specific hardware:

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- Accelerates processing bottlenecks (“hotspots”),
- Not reusable in general,
- Not scalable in general,
- Introduces co-design problem.

Reconfigurable hardware

Create “virtual hardware” devices on one reprogrammable array.

- Adapt to mode changes,

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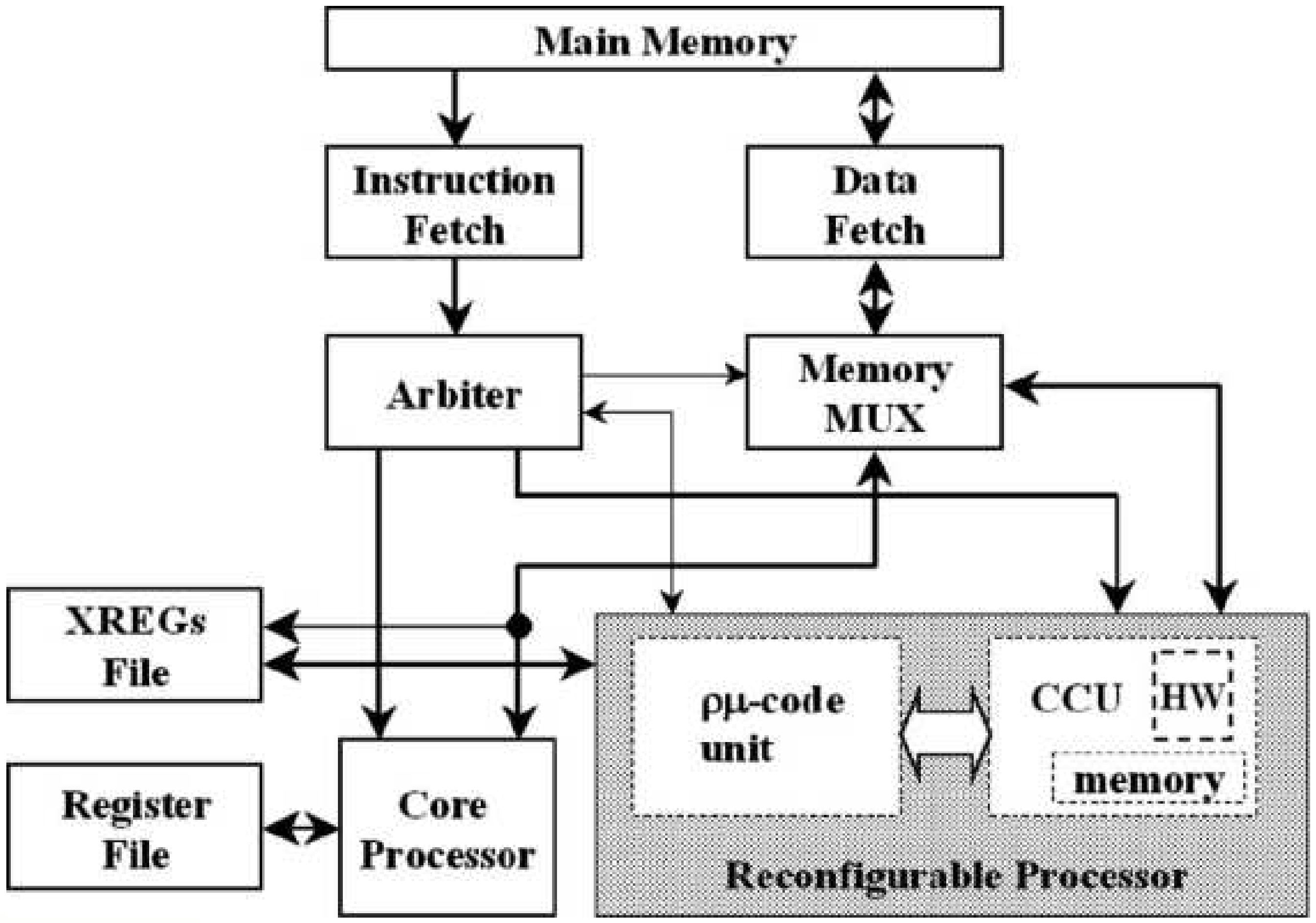
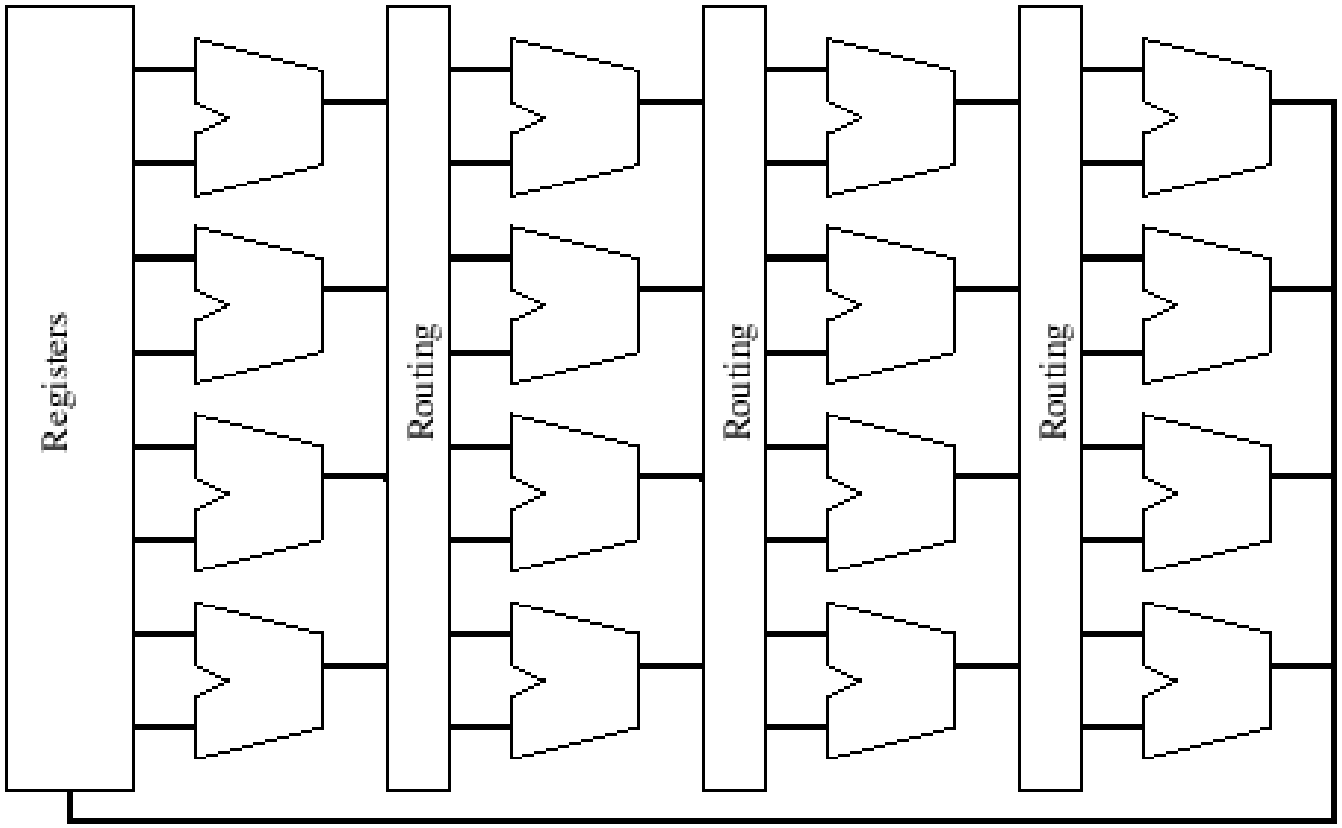
- Introduces **compatibility** problem,
- Introduces **predictability** problem.

Fine-grained array [25]



Coarse-grained array [9, 24]



Proposed Solution

Microcoded **c**oarse-**g**rained **re**configurable **p**rocessor: software controlled CPU

- Based on Coarse-grained Array,

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Microcoded **c**oarse-**g**rained **re**configurable **p**rocessor: software controlled CPU

- Based on Coarse-grained Array,
- Many reprogrammable processors,
- Each can run programs from external memory and from internal microcode.

MCGREP Paradigm

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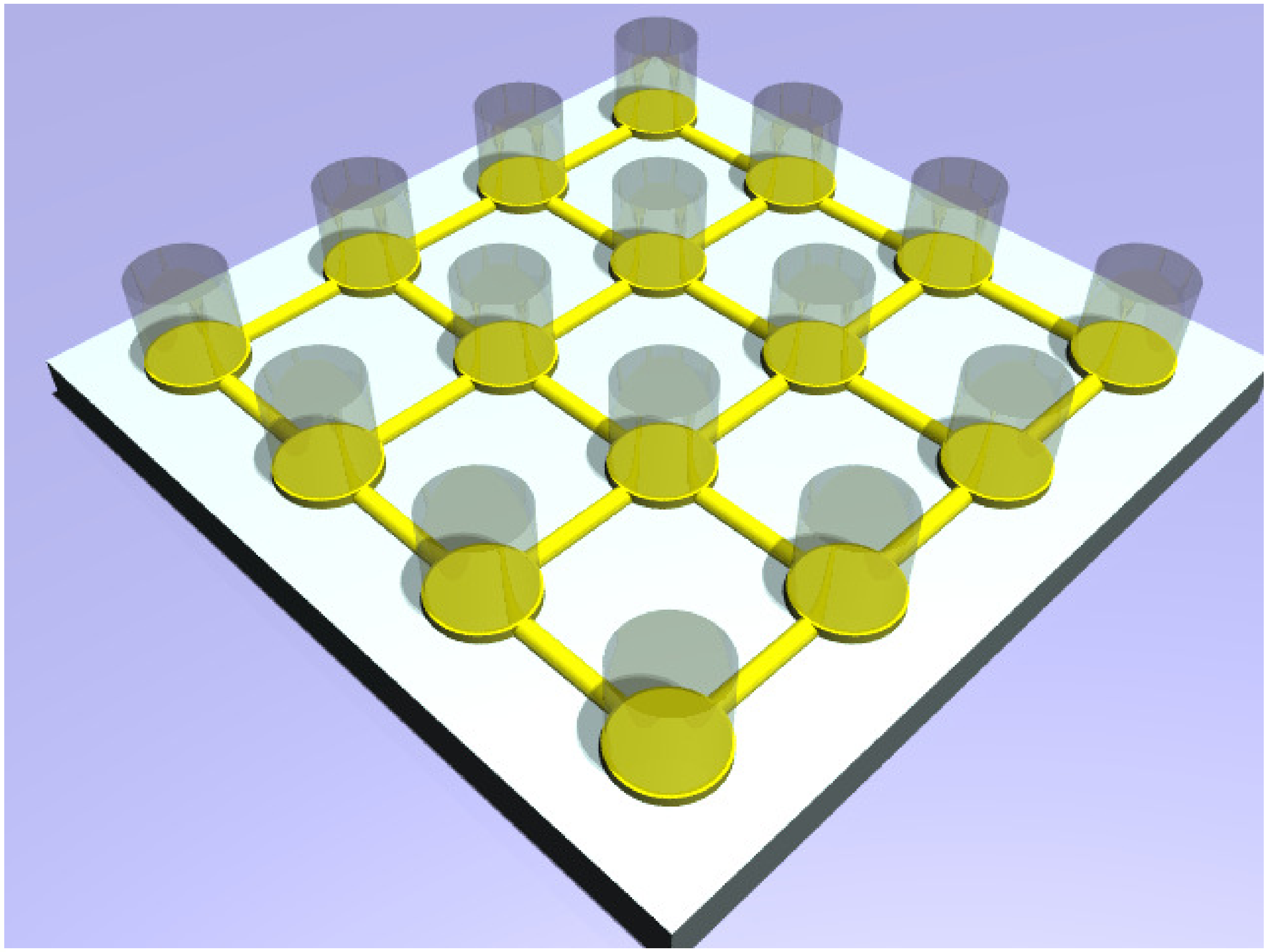
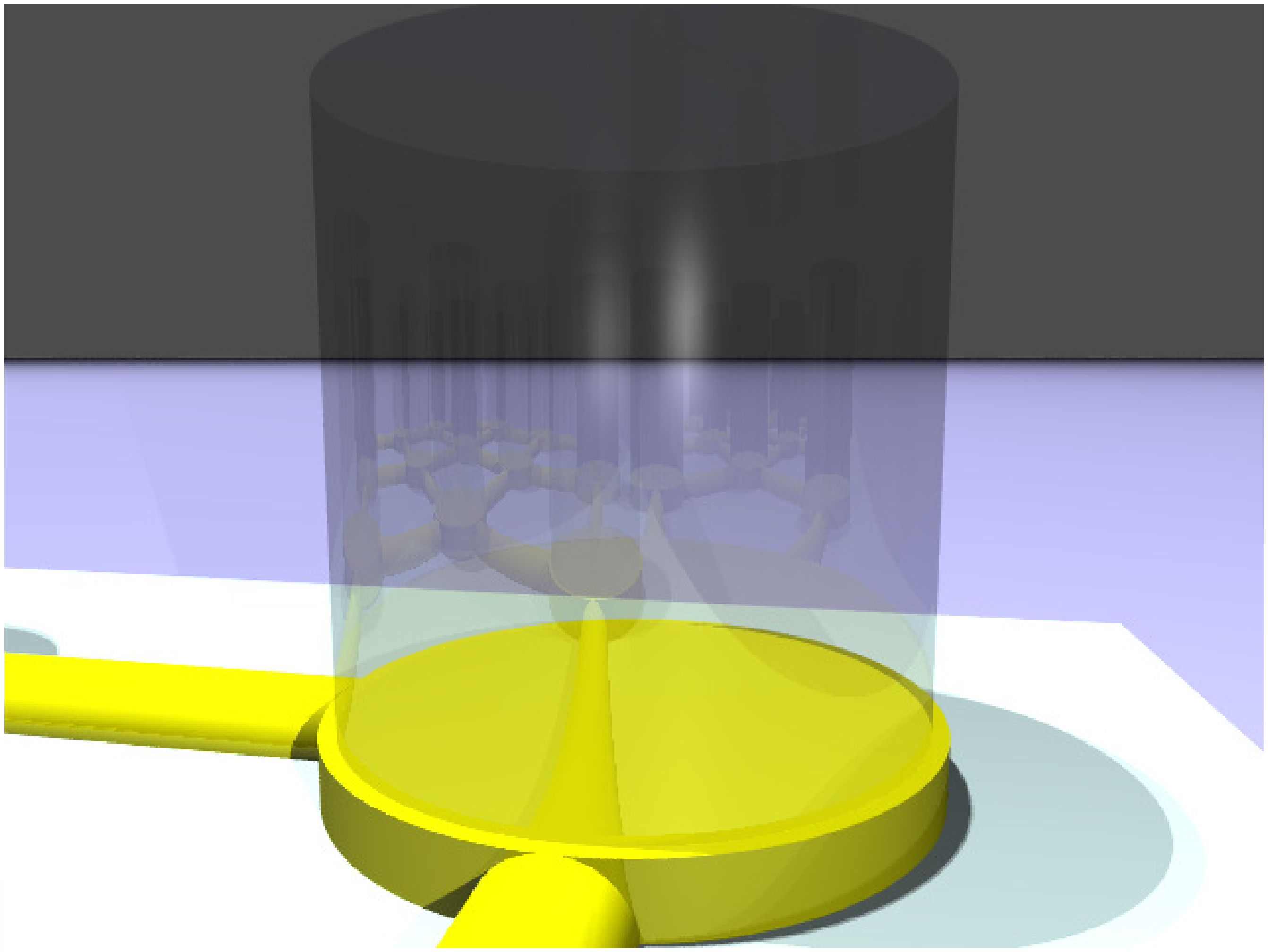
- Hotspot tasks are distributed to all or part of the reconfigurable array.
- ILP exploited as multiple processors may be used to execute each task.
- Applications are speeded up!
- Predictability and scalability retained.

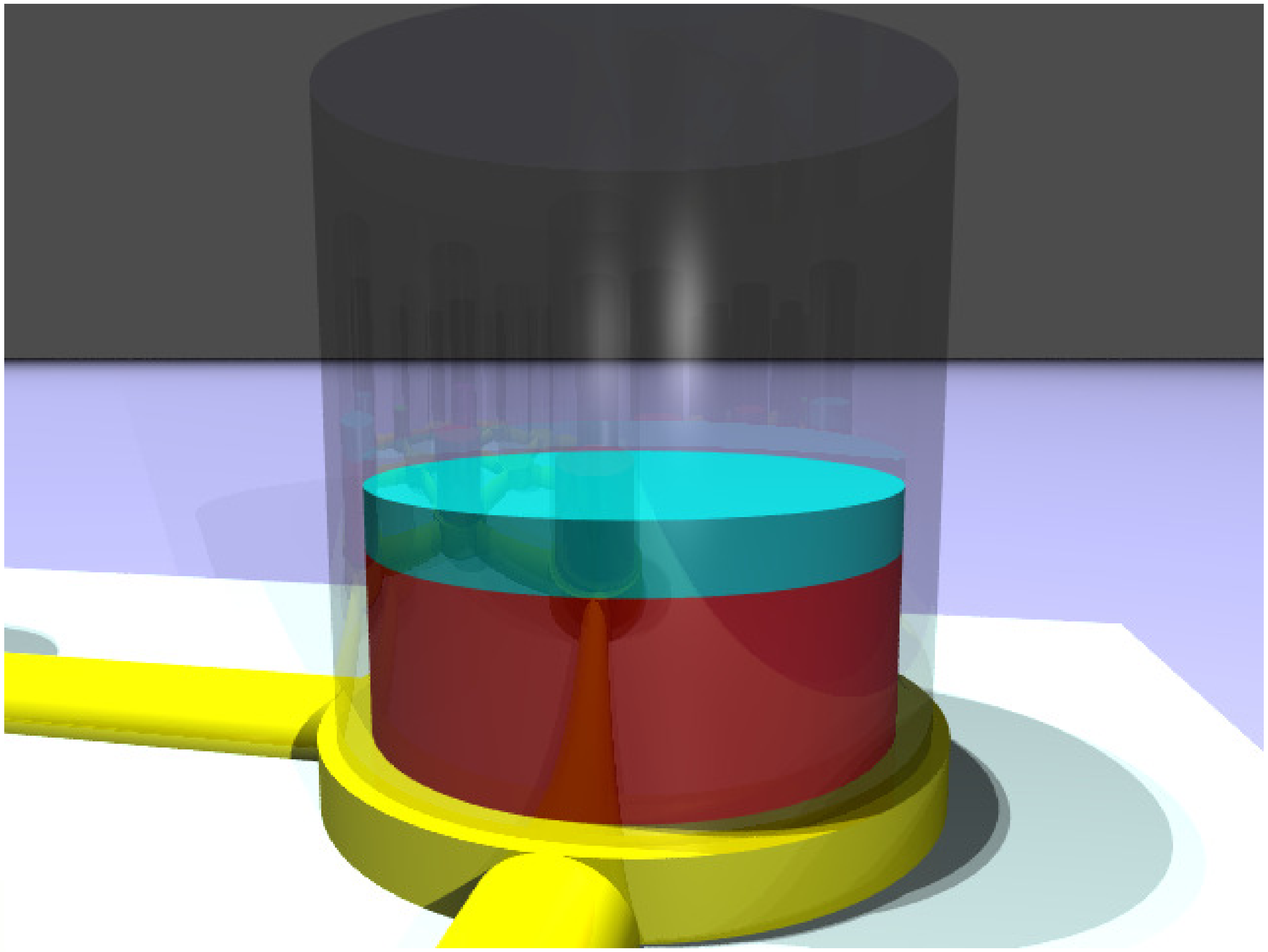
Distributing Applications (1)



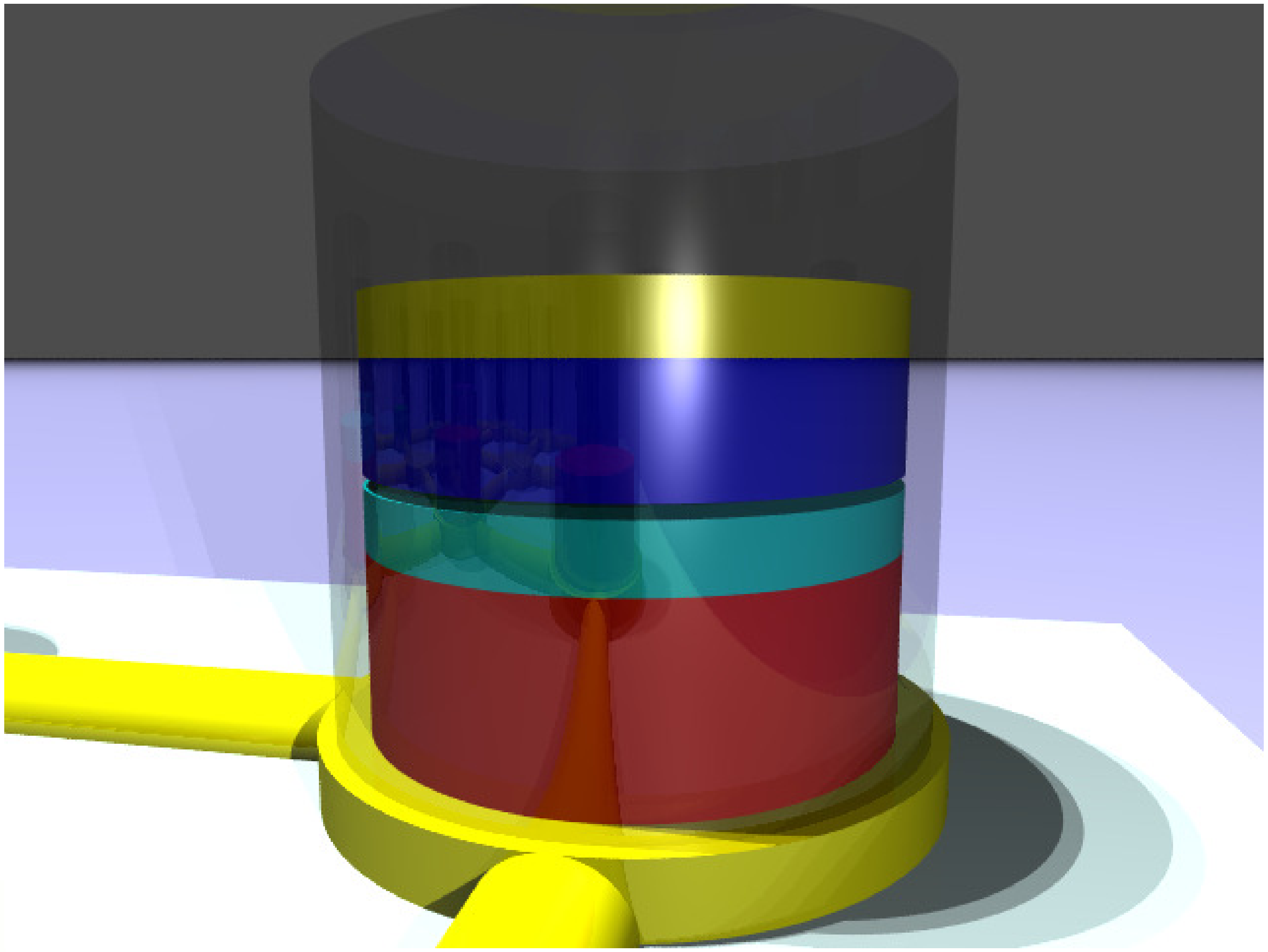
Distributing Applications (2)



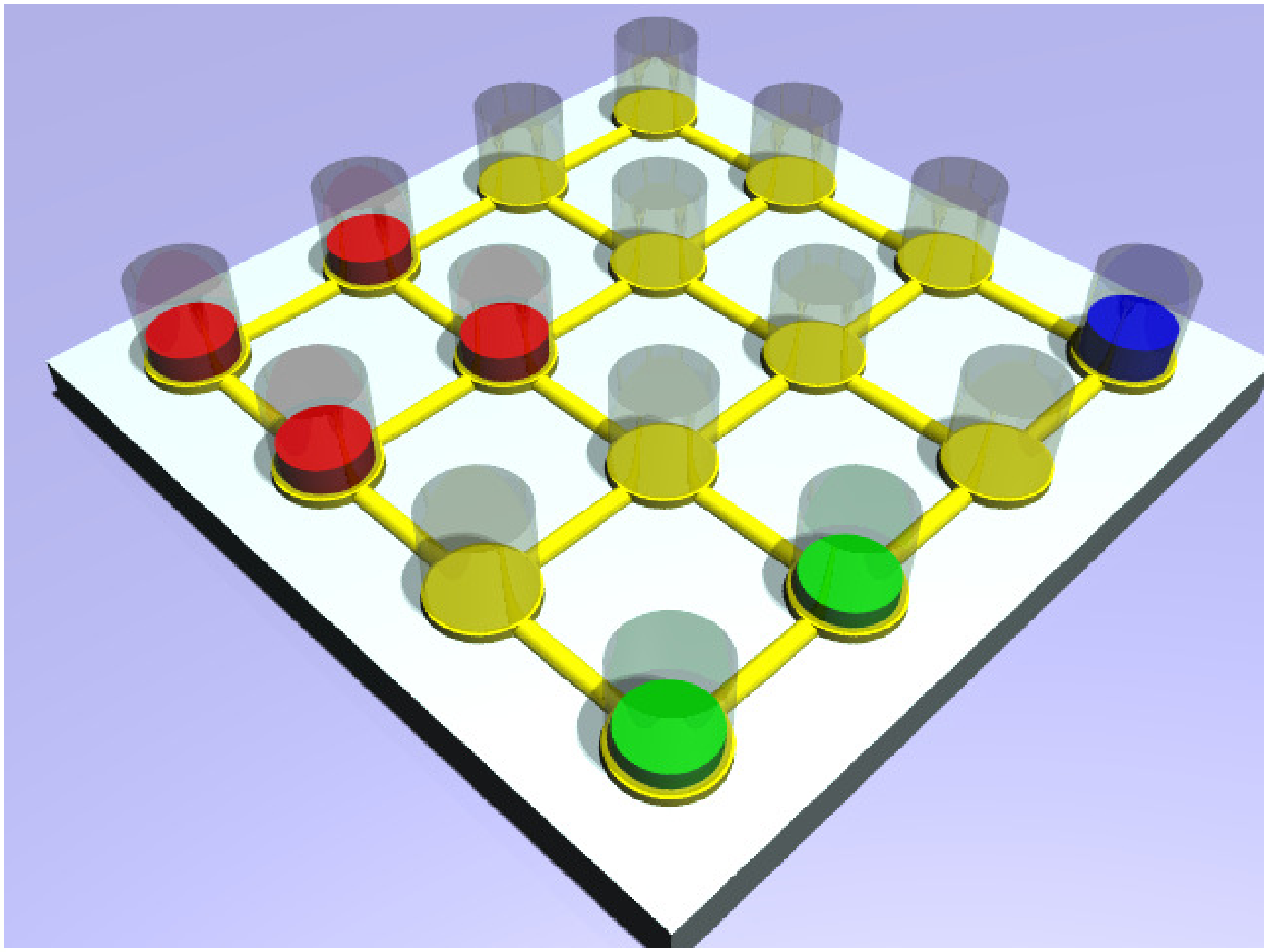
Distributing Applications (3)



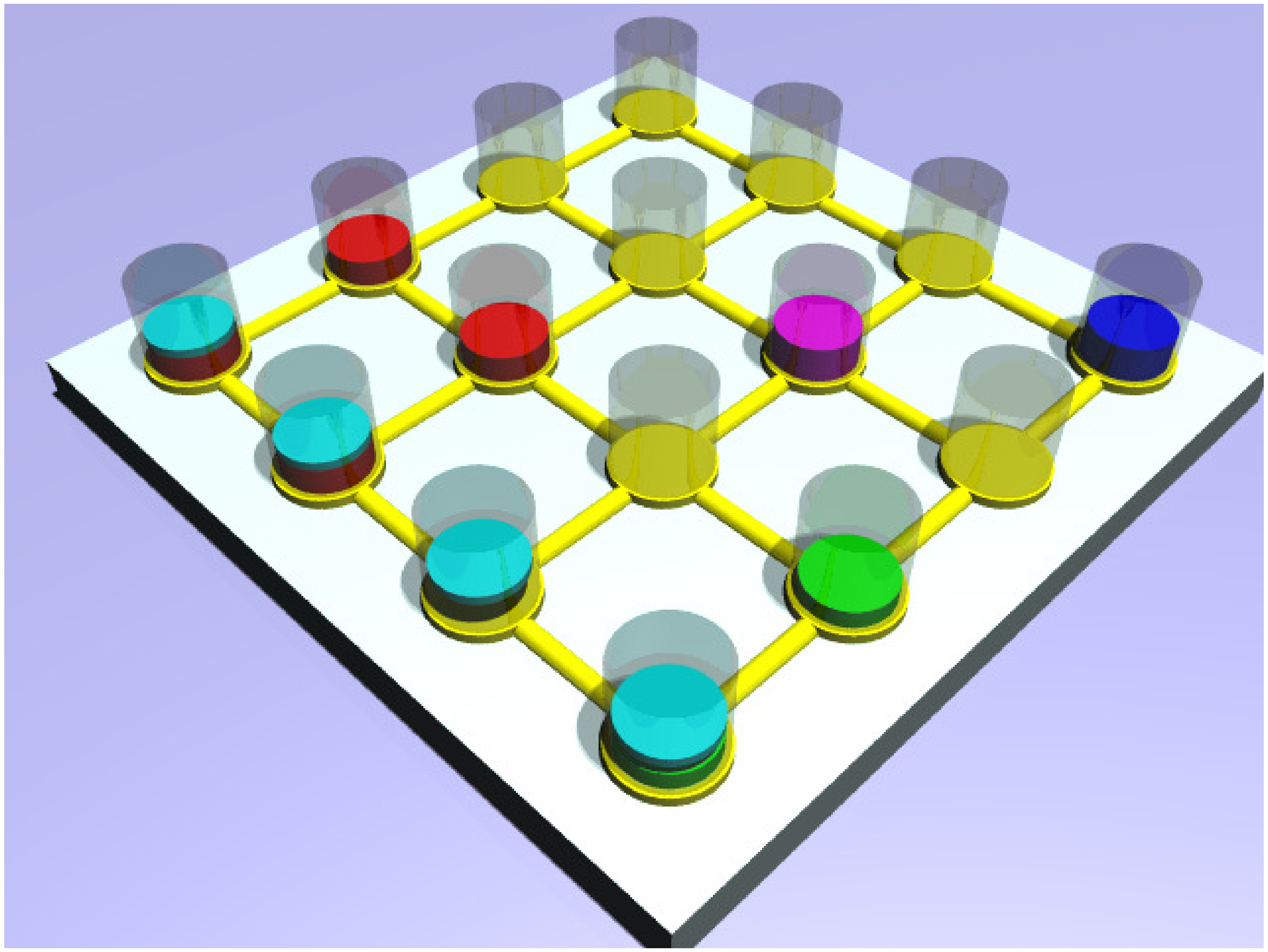
Distributing Applications (4)



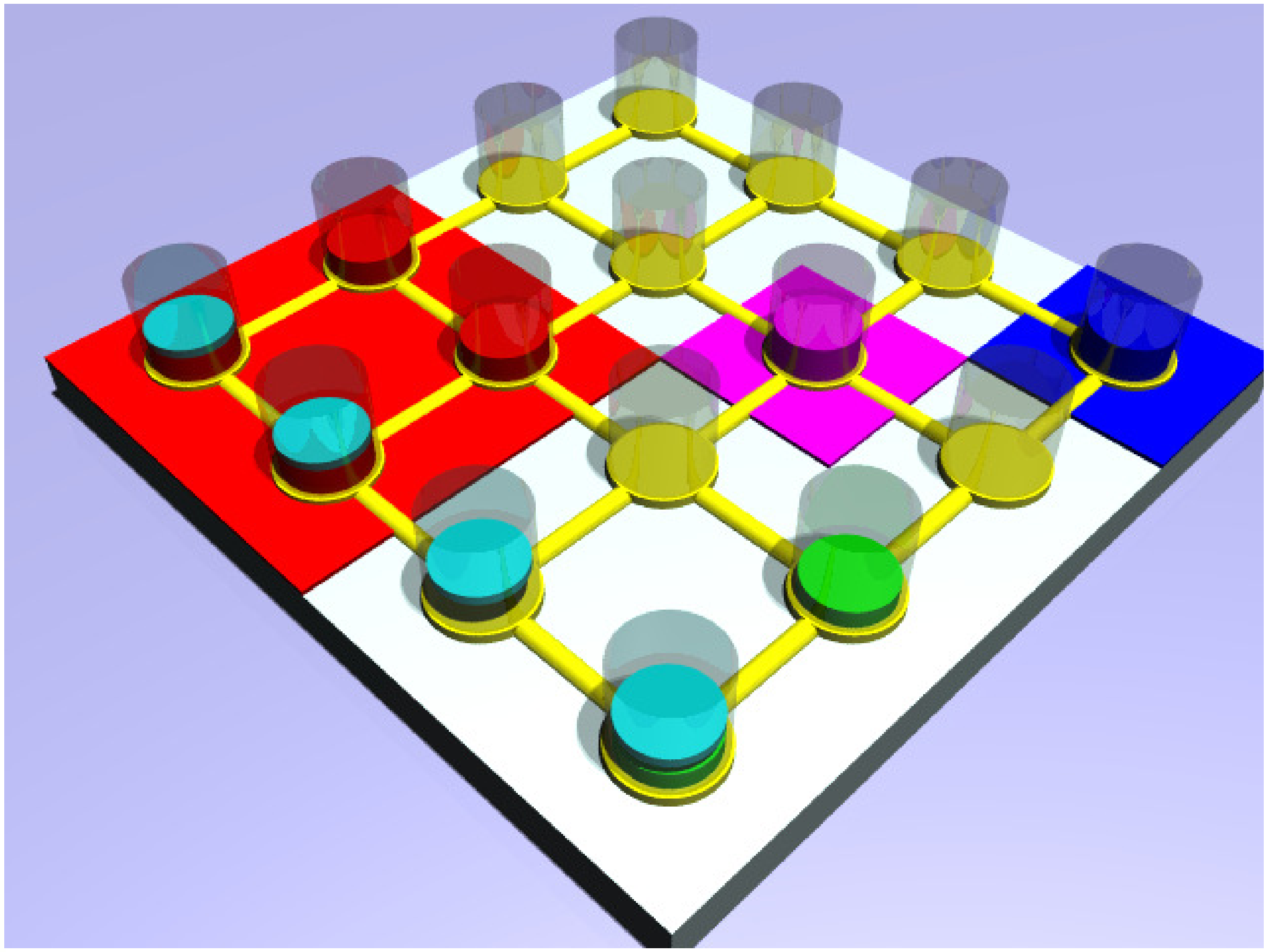
Distributing Applications (5)



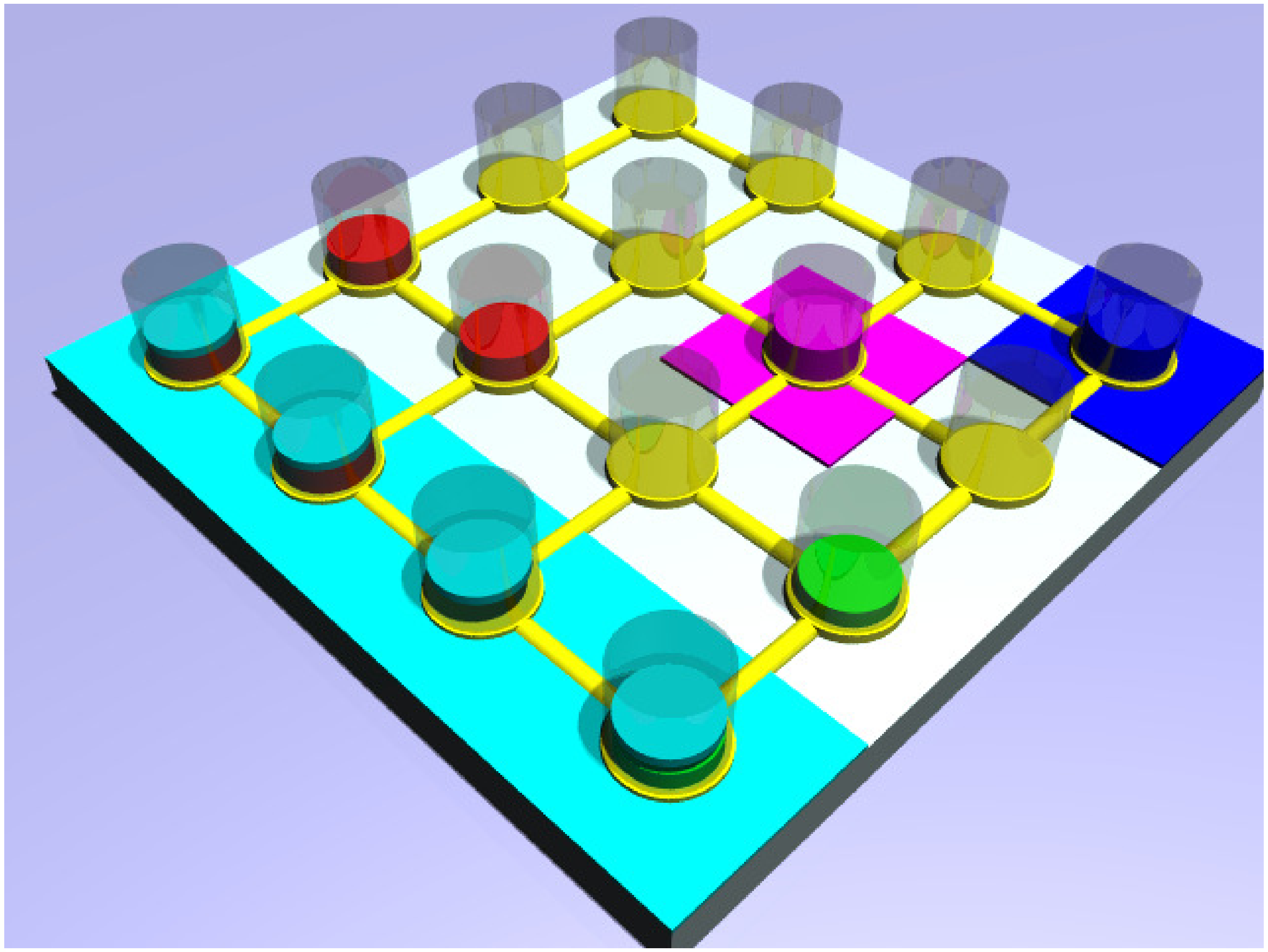
Distributing Applications (6)



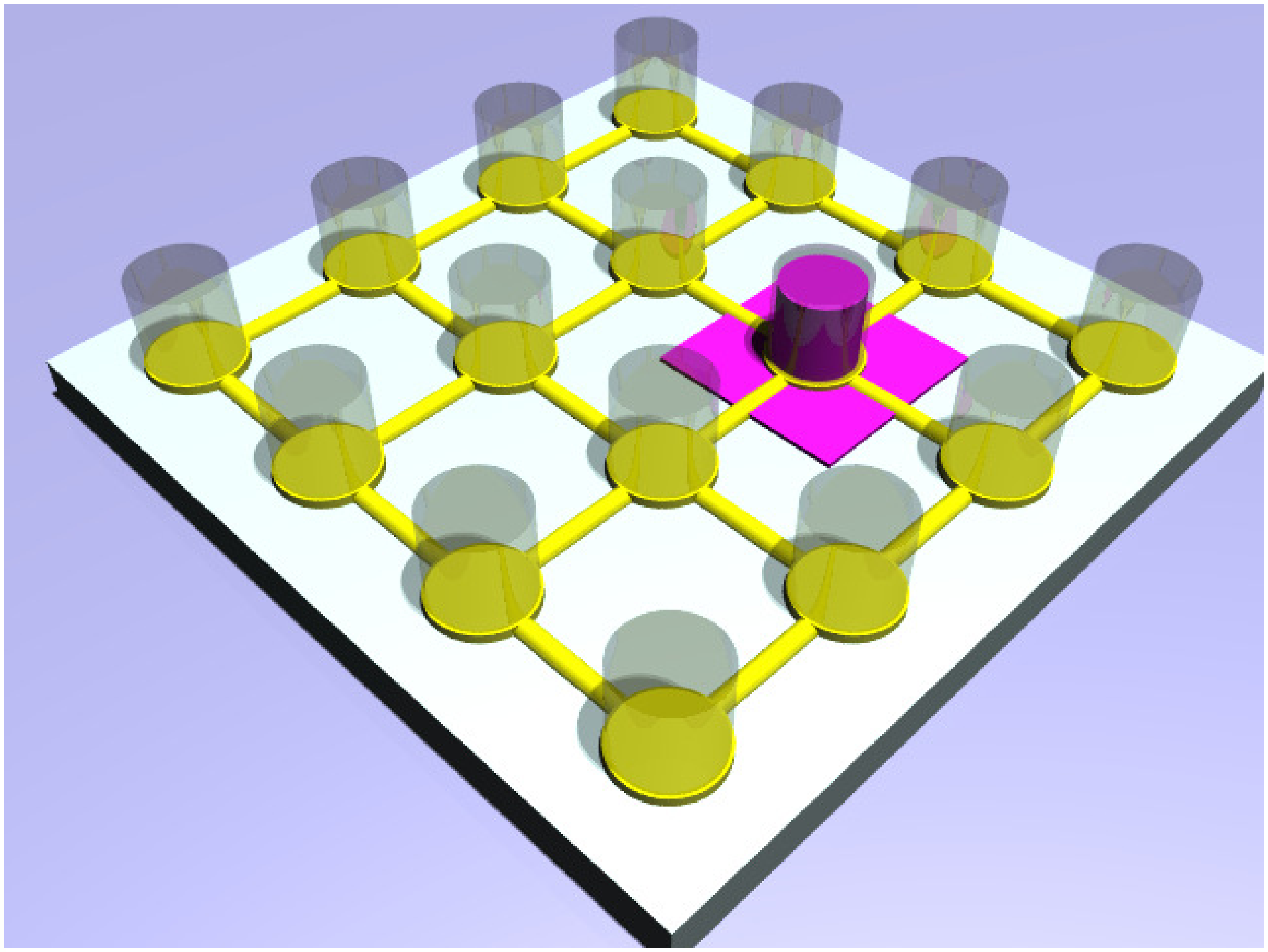
Distributing Applications (7)



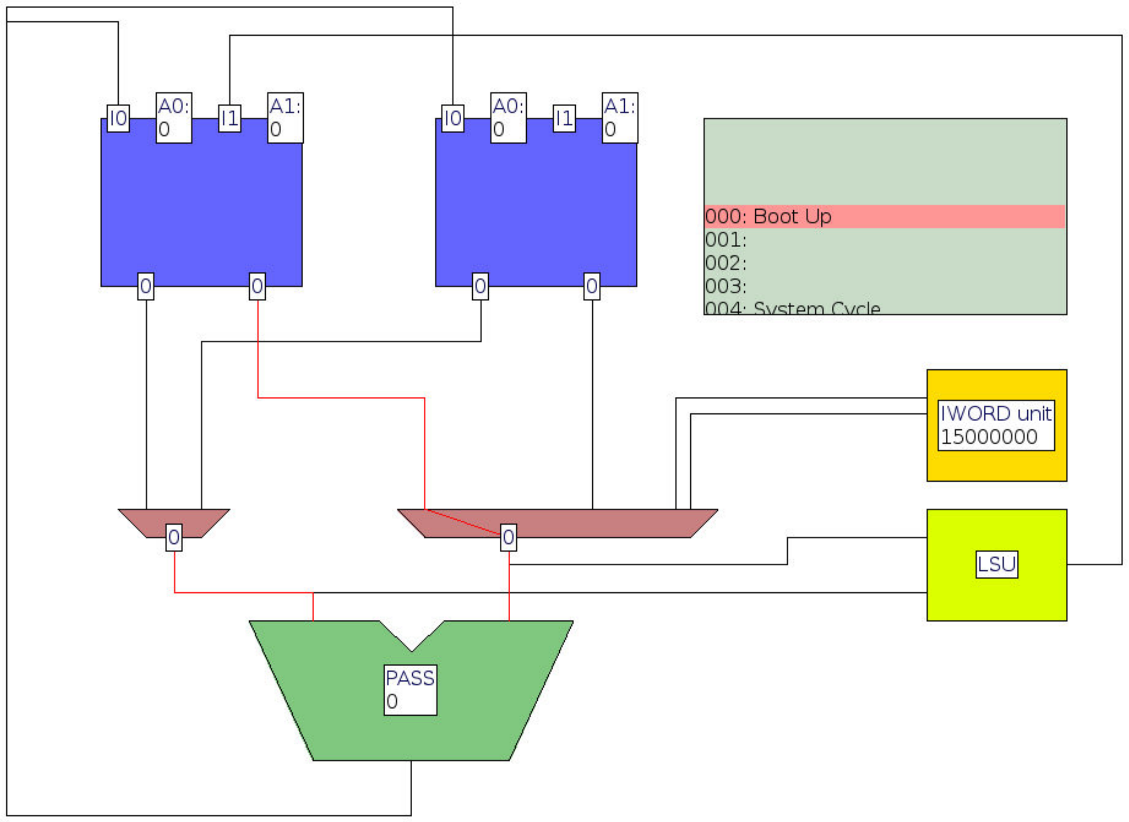
Distributing Applications (8)



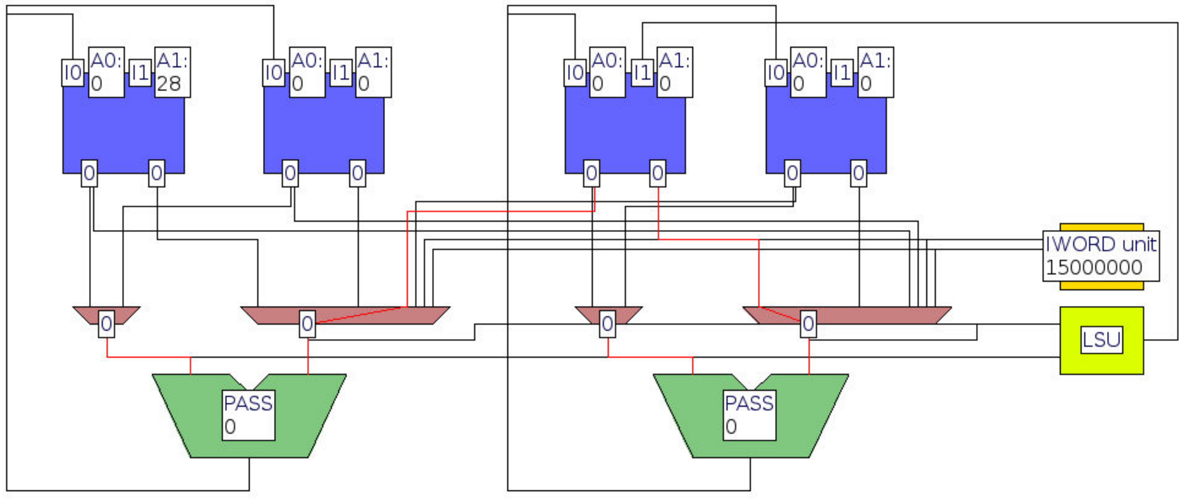
Distributing Applications (9)



How it works


I0
A0:
0
I1
A1:
0
I0
A0:
0
I1
A1:
0
0
0
0
0
000: Boot Up
001:
002:
003:
004: System Cycle
IWORD unit
15000000
0
0
LSU
PASS
0

How it works



000: Boot Up
001:
002:
003:
004: System Cycle
005: Reenter Machine Code

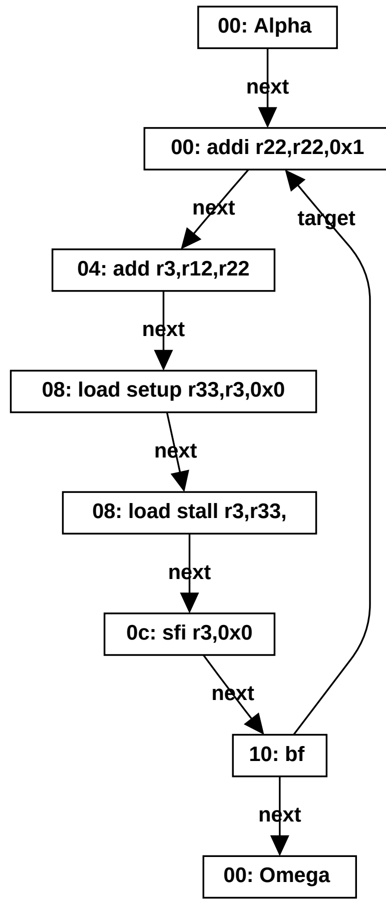
Making microcode

Input: **machine code**,

1. Generate operation graph,
2. Re-schedule operations to make best use of n processors,
3. Convert schedule to microcode for each processor.

Making microcode (1)

1: Generate operation graph.



```
 0: 9e d6 00 01 l.addi r22,r22,0x1
 4: e0 6c b0 00 l.add r3,r12,r22
 8: 90 63 00 00 l.lbs r3,0x0(r3)
 c: bc 23 00 00 l.sfnei r3,0x0
10: 13 ff ff fc l.bf 0x0
14: 15 00 00 00 l.nop 0x0
```

Making microcode (2)

2: Re-schedule operations to make best use of n processors.
Sample ($n = 2$):

	Node 0	Node 1
Time 0	load setup	nop
	address $\leftarrow r252$	
Time 1	load stall	nop
	$r250 \leftarrow$ output	
Time 2	add	compare
	$r254 \leftarrow r254 + 1$	$r244 \leftarrow r250 \neq 0$
Time 3	add	branch
	$r252 \leftarrow r248 + r254$	$r244$

Making microcode (3)

3: Schedule converted to microcode for each processor.

Each micro-instruction includes:

- Settings for multiplexers,
- Register file commands,
- ALU commands,
- Branch unit commands.

Sample microcode

```
              node 0                     node 1

04    16000245 03b801f9  00000200 00b80000
05    0c000245 03b801fb  00000200 00b80000
06    0cfe8245 03b801fd  00fe8245 00b801fd
07    00ff8245 03b861ff  00ff8245 00b801ff
08    00000200 03b86000  00fc824d 00b801f9
09    00000200 03b80000  00fd824d 00b801fb
0a    00000200 03b85e4e  00000200 00b80000
```

Predictability retained...

At the **microarchitecture** level...

(from Heckmann *et. al.*[10])

- No caches,

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At the **microarchitecture** level...

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- No caches, ...or at least cache replacement strategies that always lead to known states,
- No dynamic branch prediction,
- No shortcuts in hardware implementation,
- In-order execution,
- Simple pipeline.

Predictability retained...

And at the **array** level:

- Array composed of predictable parts,

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Result: No special WCET analysis difficulty is introduced.

This Implementation

Implemented on FPGA and in software simulator.

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This Implementation

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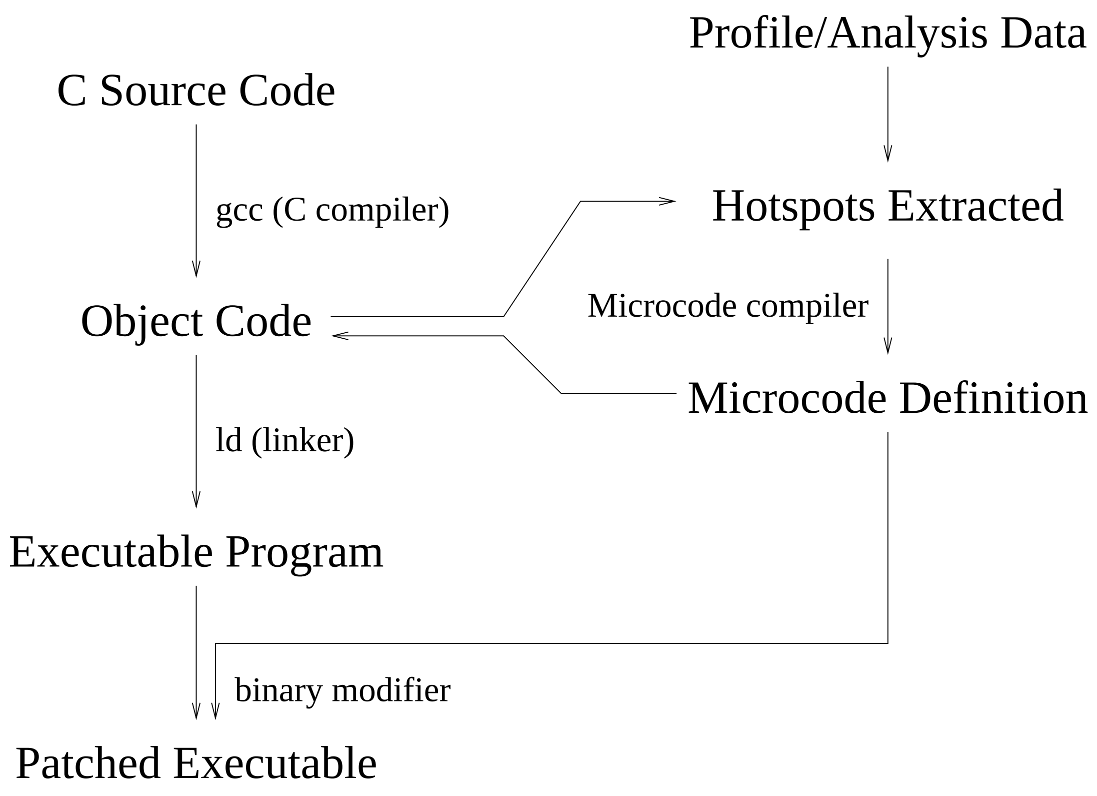
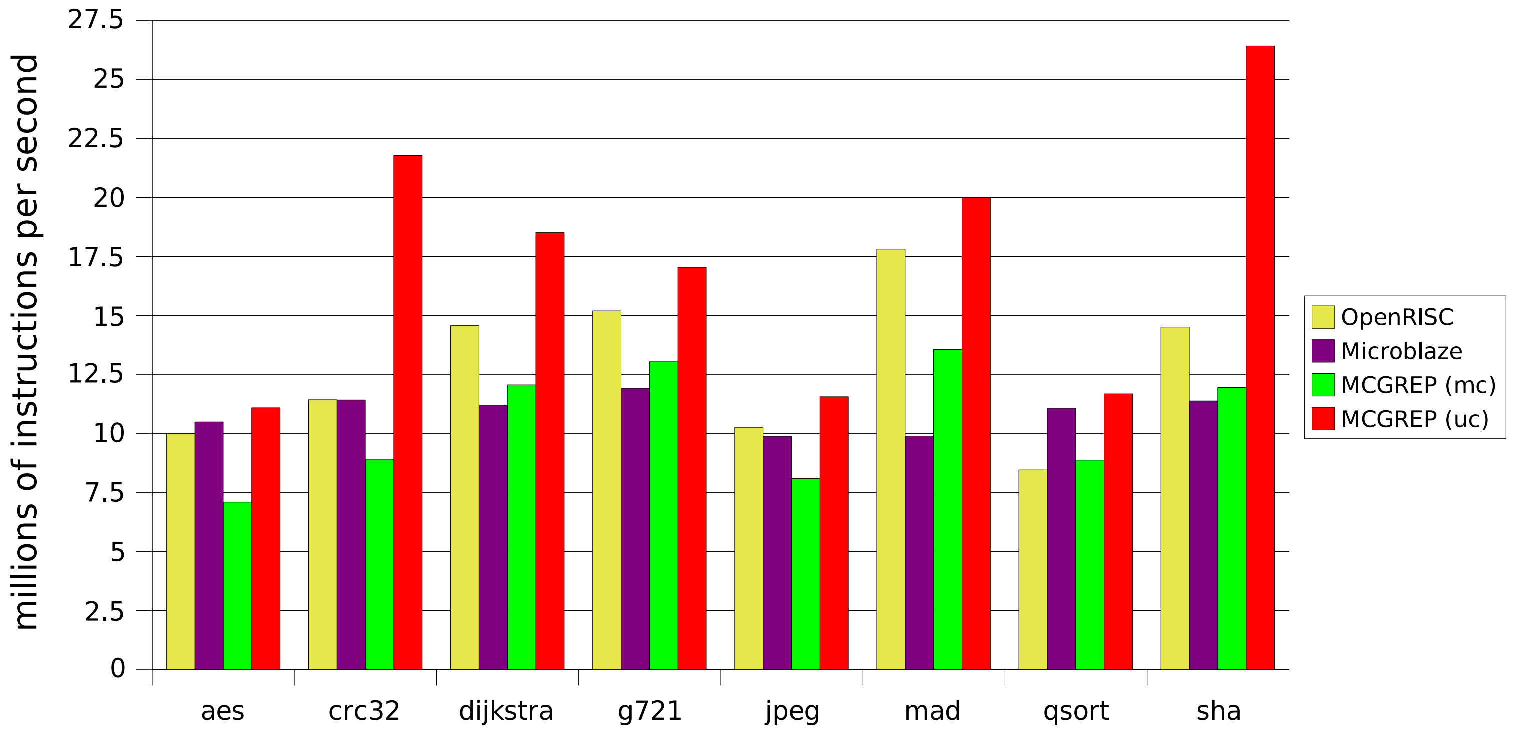
- Only two processors, permanently locked together,
- Microcode task fragments generated by partly manual process,
- No predication,
- Executes either RISC code (via interpreter microprogram) or **task fragments** written in microcode.

Toolchain


Profile/Analysis Data
C Source Code
gcc (C compiler)
Hotspots Extracted
Microcode compiler
Object Code
Microcode Definition
ld (linker)
Executable Program
binary modifier
Patched Executable

Evaluation

1. Instruction Throughput versus Hardware Size Comparison by experiment:



Evaluation

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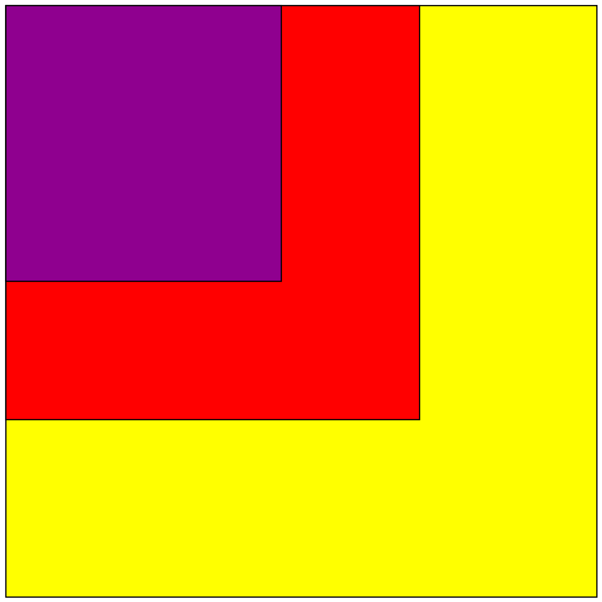
Relative FPGA areas:



🟪	Microblaze
🟥	MCGREP
🟨	OpenRISC

Evaluation

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- Task execution time independent of hardware state: all instructions have a fixed execution time.

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- Execution highly resistant to interference: experimental evidence is given in the paper.

WCET analysis does not need to track the hardware state.

Desirable Properties

There is a mechanism for generating very low level microcode from machine code...

can this be used for anything else?

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Define critical RTOS components in assembly or C, then turn them into microcode, *e.g.*

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- Microcoded context switcher,
- Microcoded interrupt service routine,
- Any atomic operation,
- Immediate priority ceiling protocol.

Paper includes example microcode for these.

Conclusion

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Future plans - to experiment with...

- Larger versions of architecture,
- Multitasking, dynamic compilation and 2D scheduling.

Questions?

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